

CLAIMS

What is claimed is:

1. A method for reducing the loss of silicon in a plasma assisted photoresist etching process comprising the steps of:

providing a silicon substrate including a polysilicon gate structure;

masking a portion of the silicon substrate with photoresist to carry out an ion implantation process for forming source and drain regions;

carrying out an ion implantation process; and,

removing the photoresist according to at least one plasma assisted process comprising fluorine containing, oxygen, and hydrogen containing plasma source gases.

2. The method of claim 1, wherein the at least one plasma assisted process comprises a single plasma etching process whereby fluorine containing, oxygen, and hydrogen containing plasma source gases are simultaneously provided.

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3. The method of claim 2, wherein the single etch process includes plasma source gases consisting essentially of a fluorocarbon, oxygen, hydrogen, and an inert gas.

4. The method of claim 3, wherein the single etch process includes plasma source gases consisting essentially of a CF_4 , O_2 , H_2 , and N_2 .

5. The method of claim 4, wherein the N_2 and H_2 are provided having a volumetric ratio of N_2 to H_2 of about 10 to 1 to about 1 to 10.

6. The method of claim 1, wherein the at least one plasma assisted etching process is carried out at a zero RF bias.

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7. The method of claim 1, wherein the at least one plasma assisted process comprises at least one sequential etch/plasma treatment/etch process wherein the etch process comprises at least one of a fluorocarbon/oxygen and fluorocarbon/oxygen/hydrogen/inert gas chemistry and the plasma treatment process comprises a hydrogen/inert gas chemistry.

8. The method of claim 7, wherein the hydrogen/inert gas chemistry consists essentially of a N_2 and H_2 provided having a volumetric ratio of N_2 to H_2 of about 10 to 1 to about 1 to 10.

9. The method of claim 1, wherein a silicon oxide layer is provided over the silicon substrate prior to the ion implantation process.

10. The method of claim 1, wherein an amorphous silicon region is created at the silicon surface following the ion implantation process.

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11. A method for reducing the loss of silicon over source and drain regions in a CMOS device in a plasma assisted photoresist etching process comprising the steps of:

providing an exposed silicon oxide layer over a silicon substrate adjacent a polysilicon gate structure comprising adjacent sidewall spacers;

masking a portion of the exposed silicon oxide layer with photoresist to carry out an ion implantation process for forming source and drain regions within the silicon substrate;

carrying out an ion implantation process to form source and drain regions within the silicon substrate including partially amorphizing the source and drain regions to create coordinatively unsaturated silicon bonds; and,

removing the photoresist according to a plasma assisted process comprising fluorine containing, oxygen, and hydrogen containing plasma source gases to coordinately saturate at least a portion of the coordinatively unsaturated silicon bonds.

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12. The method of claim 11, wherein the plasma source gases consist essentially of at least one fluorocarbon, oxygen, hydrogen, and an inert gas.

13. The method of claim 12, wherein the plasma source gases consist essentially of CF_4 , O_2 , H_2 , and N_2 .

14. The method of claim 13, wherein N_2 and H_2 are provided having a volumetric ratio of N_2 to H_2 of about 10 to 1 to about 1 to 10.

15. The method of claim 11 wherein plasma assisted etching process operating conditions comprise operating pressures of from about 5 milliTorr to about 100 milliTorr, an RF power of about 200 Watts to about 1000 Watts, and an adjustably decoupled RF bias power of about 0 Watts to about 100 Watts.

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16. The method of claim 14, wherein the plasma assisted process operating conditions comprise a CF_4 flow rate of about 30 sccm to about 100 sccm, an O_2 flow rate of from about 3000 sccm to about 5000 sccm, and a combined flow rate of N_2 and H_2 of from about 100 sccm to about 300 sccm.

17. The method of claim 15, wherein the at least one plasma assisted etching process is carried out at a zero RF bias power.

18. The method of claim 11, wherein the plasma assisted etching process further comprises in-situ periodic plasma treatments wherein the plasma source gases consist essentially of an inert gas and H_2 gas.

19. The method of claim 18, wherein the plasma source gases consist essentially of a N_2 and H_2 provided having a volumetric ratio of N_2 to H_2 of about 10 to 1 to about 1 to 10.

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20. The method of claim 11, further comprising carrying out at least one annealing process to at least partially recrystallize the source and drain regions.